國立彰化師範大學 102 學年度碩士班招生考試試題

系所：資訊工程學系　　科目：作業系統及計算機組織

☆☆請在答案紙上作答☆☆　　

一、 The semaphore ***mutex*** and ***wrt*** are initialized to 1; ***readcount*** is initialized to 0. The ***mutex*** semaphore is used to ensure mutual exclusion when the variable ***readcount*** is updated. Please complete the following code for a reader process of the first readers-writers problem. **(10%)**

```
do {
    wait(wrt) ;
    …
    //writing is performed
    …
    signal(wrt) ;
} while (TRUE);
```

Figure 1. The structure of a writer process

```
do {
    wait(mutex) ;
    readcount++ ;
    if (readcount = = (1) )
        (2) ;
    signal(mutex) ;
    …
    //reading is performed
    …
    wait(mutex) ;
    (3) ;
    if (readcount = = (4))
        (5) ;
    signal(mutex) ;
} while (TRUE);
```

Figure 2. The structure of a reader process.

二、 Consider the parameter △ used to define the size of working-set window in the working-set model. What is the effect of setting △ to a small value on the page-fault frequency and the number of active (nonsuspended) process currently executing in the system? What is the effect when △ is set to a very high value? **(10%)**

三、 Suppose that a scheduling algorithm (at the level of short-term CPU scheduling) favors those process that have used the least processor time in the recent past. Why will this algorithm favor I/O-bound programs and yet not permanently starve CPU-bound programs? **(10%)**

四、Explain the difference between internal and external fragmentation. **(10%)**

五、Typically, at the completion of a device I/O, a single interrupt is raised and appropriately handled by the host processor. In certain settings, however, the code that is to be executed at the completion of the I/O can be broken into two separate pieces. The first piece executes immediately after the I/O completes and schedules a second interrupt for the remaining piece of code to be executed at a later time. What is the purpose of using this strategy in the design of interrupt handlers? **(10%)**

六、Answer the following questions. **(50%)**

(a) In measuring the CPU performance of a computer, what does *CPI* mean? Let *N* be the instruction count of a program and *T* be the clock cycle, how to determine the CPU time spent on this program?

(b) In the MIPS architecture, what are *data transfer instructions*? What kind of instruction belongs to this type?

(c) There are 32 registers in the MIPS architecture. Please explain the meaning of register $zero. How to use an **add** instruction to copy the value stored in register $t1 to register $t2?

(d) The **jal** instruction is usually used during procedure call. Please explain the meaning of this instruction. How to return the result (in hardware) after procedure call?

(e) Sign extension is a technique to convert a binary number represented in *n* bits to a number represented with more than *n* bits. Please convert 4-bit binary versions of 3 and -3 to 8-bit binary numbers.

(f) Compared with the single cycle design of the MIPS architecture, what are the two advantages of a multicycle design?

(g) In a computer pipeline, data hazards arise from the dependence of one instruction on an earlier one that is still in the pipeline. Give a solution to this hazard from the viewpoint of hardware and software, respectively.

(h) For the IEEE 754 single-precision format, find the single-precision representation of a decimal number 0.375.

(i) A memory hierarchy consists of multiple levels of memory with different speeds and sizes. In the memory hierarchy design, what is the principle of spatial locality? How to apply this principle to the design of caches?

(j) In the virtual memory design, the main memory acts as a *cache* for the secondary storage (usually implemented with magnetic disks). Please explain the meaning of virtual address. How to access physical memory from this address?