國立彰化師範大學 100 學年度碩士班招生考試試題

系所：資訊工程學系　　科目：作業系統及計算機組織

☆☆請在答案紙上作答☆☆　　

1. Which of the following components of a program state are shared across threads in a multithreaded process. **(5%)**
   1. Register values　　2. Heap memory
   3. Global variables　　4. Stack memory

2. Please fill the blank in Figure 1 with the following items. **(8%)**
   a. I/O request　　**b**. Idle　　**c**. I/O interrupt processing
   d. Transferring　　**e**. User process executing　　**f.** Transfer done

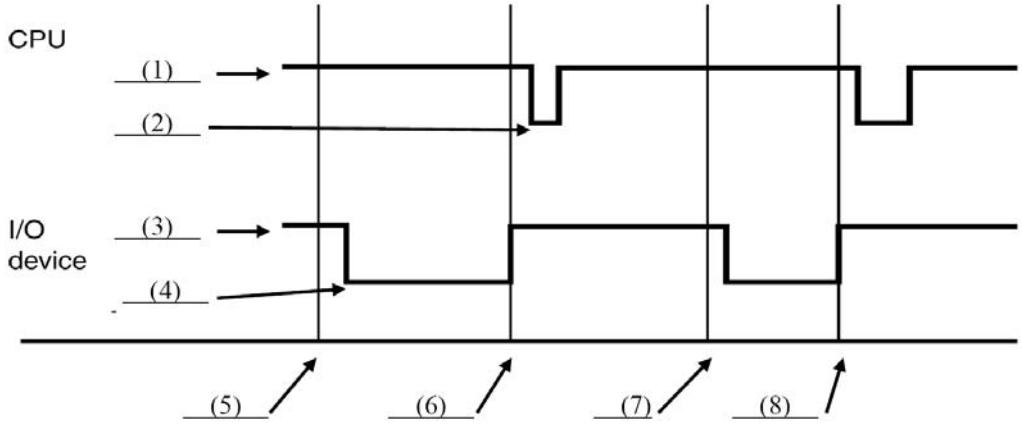

Figure 1 Interrupt time line for a single process doing output.

3. Consider a file system on a disk that has both logical and physical block sizes of 512 bytes. Assume that the information about each file is already in memory. For each of the three allocation strategies (contiguous, linked allocation, and indexed), answer these questions:
   a. How is the logical-to-physical address mapping accomplished in this system? (For the indexed allocation, assume that a file is always less than 512 blocks long)**(9%)**
   b. If we are currently at logical block 10 (the last block accessed was block 10) and want to access logical block 4, how many physical blocks must be read from the disk? **(6%)**

4. Suppose that the following processes arrive for execution at the times indicated. Each process will run the listed amount of time. In answering the questions, use nonpreemptive scheduling and base all decisions on the information you have at the time the decision must be made.

Process	Arrival Time	Burst Time
P_1	0.0	8
P_2	0.4	4
P_3	1.0	1

a. What is the average turnaround time for these processes with the first- come first-served (FCFS) scheduling algorithm. **(4%)**

b. What is the average turnaround time for these processes with the shortest-job-first (SJF) scheduling algorithm? **(4%)**

c. The SJF algorithm is supposed to improve performance, but notice that we chose to run process P_1 at time 0 because we did not know that two shorter processes would arrive soon. Compute what the average turnaround time will be if the CPU is left idle for the first 1 unit and then SJF scheduling is used. Remember that processes P_1 and P_2 are waiting during this idle time, so their waiting time may increase. This algorithm could be known as future-knowledge scheduling.**(4%)**

5. What are the differences between deadlock prevention and deadlock avoidance**. (10%)**

6. Determine if each of the following statements is true (T) or false (F). **(10%)**

(a) The number of variables in many programs is larger than that of registers in computers.The compiler tries to keep the most frequently used variables in memory and places the rest in registers.

(b) Pseudo-instructions are variations of assembly language instructions. They need not be implemented in hardware.

(c) In the MIPS instructions, the R-type and I-type instructions can be distinguished by the 6-bit op field of an instruction.

(d) Pipelining does not reduce the latency of a single task, but it improves the throughput of an entire workload.

(e) In the memory hierarchy design, if the hit rate is high enough, the memory hierarchy has an effective access time close to that of the slowest level and a size equal to that of the smallest level.

7. Explain the following terms. **(15%)**

(a) PC-relative addressing

(b) Structural pipeline hazard

(c) Branch prediction

(d) Fully associative cache

(e) Page table

8. Answer the following questions. **(15%)**

(a) Suppose a program runs in 100 seconds on a computer, with 80 seconds of multiple operations of this time. How much improvement do you have to increase the speed of multiplication if you want the program to run four times faster?

(b) For an array *A* stored in memory, write a MIPS instruction to load the value of *A*[3] into register $t1. Assume byte addressing is used here and the base address of *A* is stored in register $s1.

(c) When the jal (jump-and-link) instruction is executed, it will jump to an address and simultaneously save the address of the following instruction in $ra. What is the purpose for this address saving?

(d) Why does the IEEE 754 floating-point standard use a bias of 127 for single precision and 1023 for double precision?

(e) Compared with the single-cycle design, what is the advantage of a multicycle design?

9. Shown in Figure 2 is the datapath for execution of an R-type instruction "add $t1, $t2, $t3". Describe the four steps in executing this instruction. **(10%)**

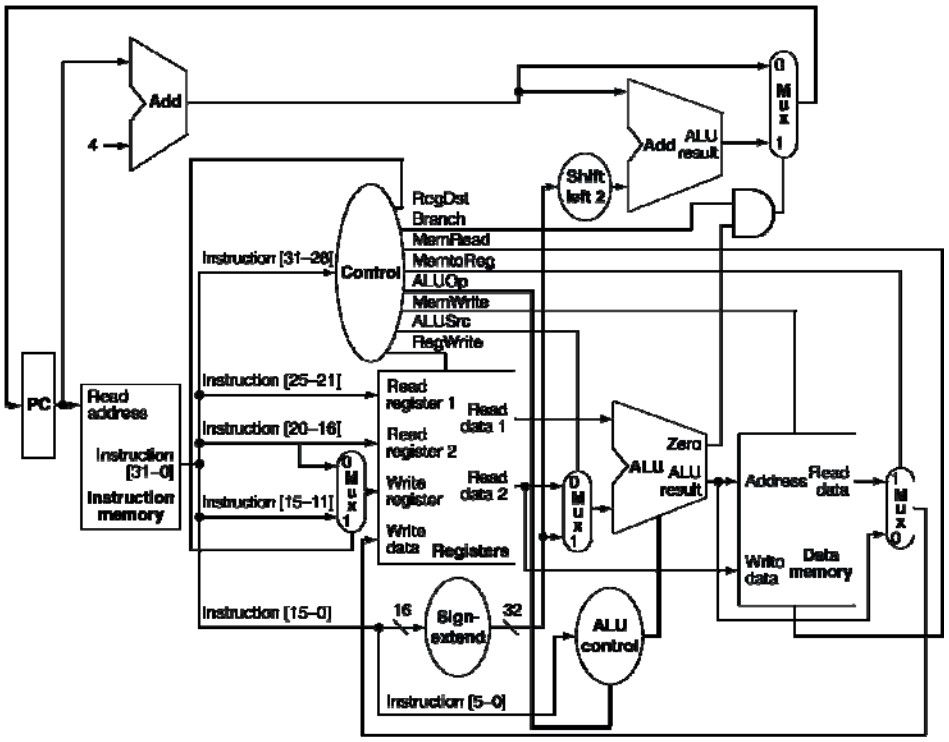

Figure 2