

國立彰化師範大學 98 學年度碩士班招生考試試題

系所：資訊工程學系

科目：作業系統及計算機組織

☆☆請在答案紙上作答☆☆

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PART I. (50%)

1. Assume that you have a page-reference string for a process with m frames (initially all empty). The page-reference string has length p ; and n distinct page numbers occur in it. Answer these questions for any page replacement algorithms:
 - (1) What is a lower bound on the number of page faults? (5%)
 - (2) What is an upper bound on the number of page faults? (5%)
2. If a solution to the critical section problem is correct, it must satisfy three necessary requirements. Show that at least one of the necessary requirements is not satisfied by the following solution. (10%)

```
boolean choosing[n];
int number[n];
do{
    choosing[i]=true;
    number[i]=max(number[0], number[1],...,number[n-1])+1;
    choosing[i]=false;
    for(j=0; j<n; j++)
        {while((number[j]!=0)&&(number[j,j]<number[i,i]));
            critical section
            number[i]=0;
            remainder section
        }while(1);
```
3. What are the main advantages of virtual-machine architecture? (10%)
4. (a) What is deadlock? What are the four necessary conditions for deadlock? (5%)
(b) How does it differ from starvation? (5%)
5. Consider a system consisting of m resources of the same type being shared by n processes. Resources can be requested and released by processes only one at a time. Show that the system is deadlock free if the following two conditions hold: (10%)
 - (a) The maximum need of each process is between 1 and m resources.
 - (b) The sum of all maximum needs is less than $m+n$.

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PART II. (50%)

6. Determine if each of the following statements is true (T) or false (F). [10%: (2*5)%]

- (a) One factor that determines the performance of a machine is the instruction count, which is determined by the implementation of the processor.
- (b) By using the addi instruction along with a negative number, a subtract immediate operation can be performed.
- (c) For the multi-cycle implementation of the MIPS processor, a functional unit can be used more than once per instruction, as long as it is used in different clock cycles.
- (d) For the pipelined implementation of the MIPS processor, the performance is improved by decreasing the execution time of an individual instruction.
- (e) The design of a memory hierarchy is to present the user with as much memory as is available in the cheapest technology.

7. For the load instruction: lw \$t1, offset(\$t2), explain its five steps of execution. [10%]

8. Answer the following questions. [15%: (3*5)%]

- (a) When the jal (jump-and-link) instruction is executed, what will be done?
- (b) We know that pseudoinstructions need not be implemented in hardware, how can they be executed by hardware?
- (c) In the memory hierarchy design, what is a directed-mapped cache?
- (d) Data hazard is a type of pipeline hazard, what is a data hazard?
- (e) When handling a write request to a memory with cache, what is the write-back scheme?

9. Shown in Fig. 1 is a single-cycle implementation of the MIPS processor, answer the following questions. [15%: (3*5)%]

- (a) What does “single-cycle” mean for this MIPS implementation?
- (b) What is the purpose of sending the value of PC register to an adder?
- (c) What is the purpose of using multiple levels of decoding to generate the actual ALU control bits?
- (d) What is the purpose of performing “Shift left 2” on the output bits of “Sign extend”?
- (e) What is the purpose of sending the Zero signal of the ALU to an AND gate?

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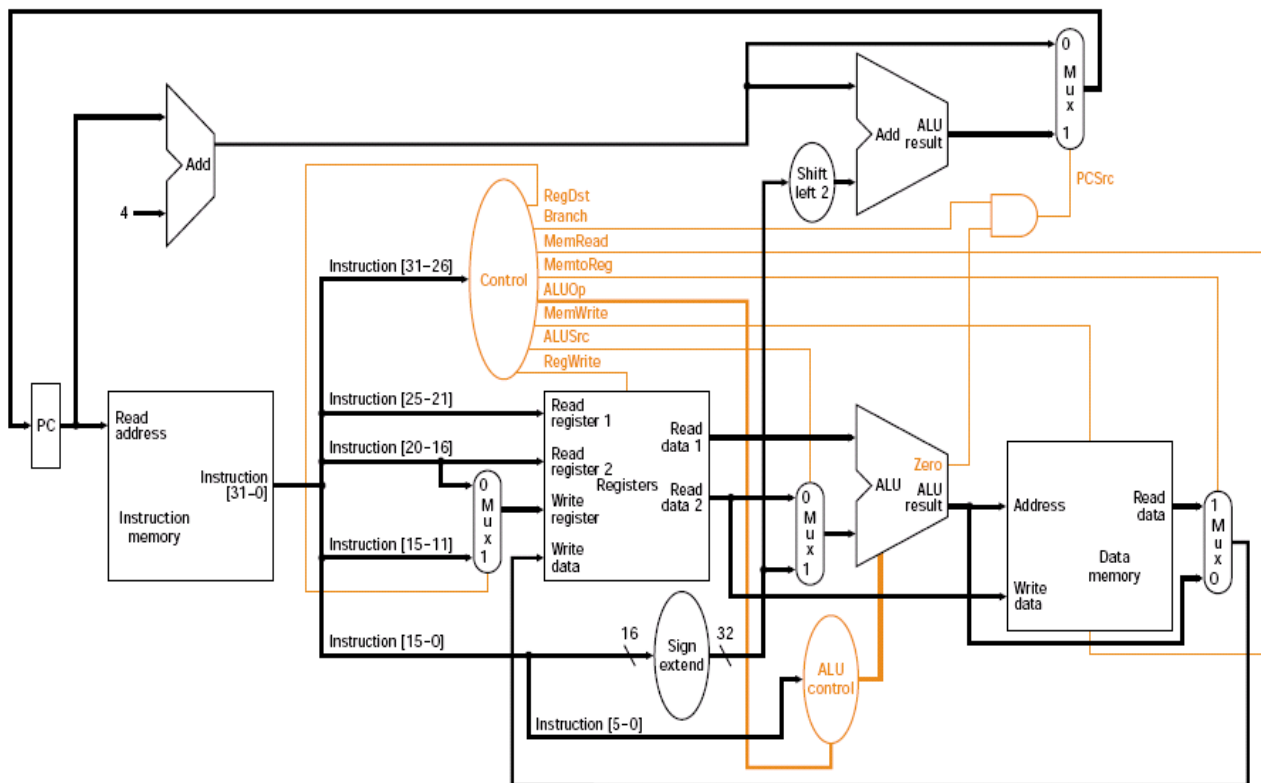


Fig. 1