國立彰化師範大學105學年度碩士班招生考試試題

系所：電子工程學系(乙組選考乙)、資訊工程學系(選考丁)、資訊工程學系積體電路設計碩士班(選考丙)　　科目：計算機組織

☆☆請在答案紙上作答☆☆　　

一、 Machine A has a clock cycle time of 40ns and an effective CPI of 1.5 for some program, and machine B has a clock cycle time of 30ns and an effective CPI of 1.2 for the same program. Which machine is faster for this program, and by how much? (10%)

二、 Suppose a program segment consists of a purely sequential part which takes 30 cycles to execute, and an iterated loop which takes 80 cycles per iteration. Assume the loop iterations are independent, and cannot be further parallelized. If the loop is to be executed 250 times, what is the maximum speedup possible using an infinite number of processors (compared to a single processor)? (10%)

三、 Translate the following two MIPS assembly instructions into 32-bit machine codes. (10%)

(a) ori R14, R28, 12
(b) sw R11, 120(R27)
[Note that R-type instruction format consists of 6 fields: op (6-bit), rs (5-bit), rt (5-bit), rd (5-bit), shamt (5-bit), and funct (6-bit); I-type instruction format consists of 4 fields: op (6-bit), rs (5-bit), rt (5-bit), and address (16-bit). The assembly instruction for LW/SW is lw/sw rt, offset(rs). The opcode of ori is 001101; The opcode of sw is 101011]

四、 Translate the following C code segment into MIPS assembly code

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for (i=0; i<10; i++)
    {if (A[i] >= B[i])
        A[i] = A[i] – B[i];
    else
        A[i] = B[i] – A[i];
    }
```

Assume variable i is already assigned to register R1, the start address of integer array A is already stored in register R21, the start address of integer array B is already stored in register R22, and assume an integer occupies 4-byte memory. (10%)

五、 Explain the meaning of MIPS instruction JAL (Jump and Link) and explain the occasion to use the JAL instruction. (10%)

六、 單選題(18%)

1. For a single-cycle design, which of the following statements is correct?
   (a) Each functional unit can be used more than once during each clock cycle.
   (b) Each instruction is broken into a series of execution steps, and each step takes one clock cycle.
   (c) Multiple instructions can be overlapped and executed concurrently.
   (d) The length of the clock cycle is the same for each instruction.
2. For a multi-cycle design, which of the following statements is correct?
   (a) The clock cycle time can be minimized by balancing the amount of work done in each cycle.
   (b) For each instruction, its CPI is equal to one.
   (c) Different instructions use the same number of clock cycles.
   (d) Different instructions can exist in the datapath at the same time and be executed concurrently.
3. For a pipelined design, which of the following statements is correct?
   (a) The lengths of the all the pipeline registers are the same.
   (b) Pipelining can decrease the execution time of an instruction when compared with the single-cycle design.
   (c) The number of overlapped instructions in the pipeline is also equal to the number of pipeline stages.
   (d) The pipeline rate is determined by the last stage in the pipeline.
4. For the pipeline hazards, which of the following statements is NOT correct?
   (a) Pipeline hazards are situations in pipelining when the next instruction cannot execute in the following clock cycle.
   (b) Structural hazard occurs when the hardware cannot support the combination of instructions that we want to execute in the same clock cycle.
   (c) Control hazard means the need to make a decision based on the result of one instruction that has already been executed and does not exist in the pipeline.
   (d) Data hazards arise from the dependence of one instruction on an earlier one that is still in the pipeline.
5. For the design of a memory hierarchy, which of the following statements is correct?
   (a) Data can be copied between any two levels at a time.
   (b) The cache in the hierarchy provides an illusion of a memory with very large size.
   (c) The hit time of the lower level is much smaller than the time to access the upper level in the hierarchy.
   (d) A level closer to the processor is generally a subset of any level further away.

6. For the virtual memory design, which of the following statements is correct?
   (a) Directed-mapped placement of pages in memory is usually adopted to reduce the page fault rate.
   (b) Having a larger number of virtual pages than number of physical pages is the basis for the illusion of an essentially unbounded amount of virtual memory.
   (c) Page faults cannot be handled in software.
   (d) Since writes take too long, the write-through scheme is usually used to save time instead of the write-back method.

七、解釋名詞(18%)

1. Program counter (PC)
2. Exception program counter (EPC)
3. Instruction throughput
4. Instruction latency
5. Cache miss
6. Page fault

八、For the single-cycle design in Fig. 1, answer the following questions. (14%)

1. Explain the results generated by functional units A (Add), B (Add), and C (Shift left 2).(8%)
2. Explain the results generated by functional unit D (ALU) for instructions **lw** and **beq**.(6%)

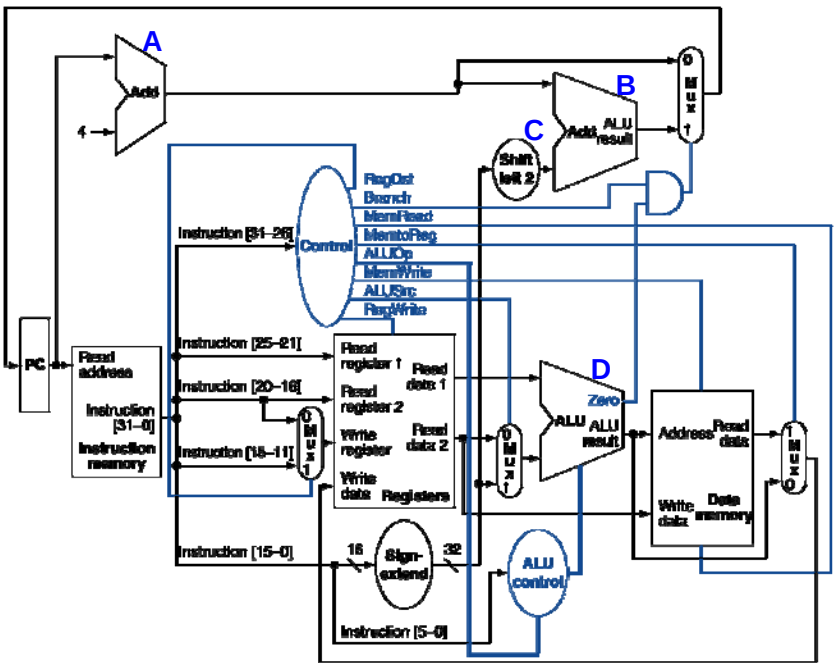

Fig. 1