國立彰化師範大學104學年度碩士班招生考試試題

資訊工程學系(選考丁)、
資訊工程學系積體電路設計碩士班(選考丙)、

系所：電子工程學系(乙組選考乙)　　科目：計算機組織

☆☆請在答案紙上作答☆☆　　

1. (10%) Assume that a design team is considering enhancing a machine by adding MMX (multimedia extension instruction) hardware to a processor. When a computation is run in MMX mode on the MMX hardware, it is 8 times faster than the normal mode of execution. Call the percentage of time that could be spent using the MMX mode the percentage of media enhancement.
   (a) What percentage of media enhancement is needed to achieve an overall speedup of 5?
   (b) What percentage of the run-time is spent in MMX mode if a speedup of 5 is achieved?

2. (10%) Computer A has an overall CPI of 1.2 and can be run at a clock rate of 500MHz.
   Computer B has a CPI of 2.5 and can be run at a clock rate of 900 MHz. We have a particular program we wish to run. When compiled for computer A, this program has exactly 100,000 instructions. How many instructions would the program need to have when compiled for Computer B, in order for the two computers to have exactly the same execution time for this program?

3. (10%) Translate the following two MIPS assembly instructions into 32-bit machine codes.
   (a) addi R11, R18, -5
   (b) lw R15, 28(R19)
   [Note that R-type instruction format consists of 6 fields: op (6-bit), rs (5-bit), rt (5-bit), rd (5-bit), shamt (5-bit), and funct (6-bit); I-type instruction format consists of 4 fields: op (6-bit), rs (5-bit), rt (5-bit), and address (16-bit). The assembly instruction for LW/SW is lw/sw rt, offset(rs). The opcode of addi is 001000; The opcode of lw is 100011]

4. (10%) Translate the following C code segment into MIPS assembly code

```
for (i=0; i<10; i++)
    {if (A[i] >= 5)
        B[i] = A[i] - 3;
     else
        B[i] = A[i] + 3;
    }
```

   Assume variable i is already assigned to register R1, the start address of integer array A is already stored in register R11, the start address of integer array B is already stored in register R12, and assume an integer occupies 4-byte memory.

5. (10%) (a) Explain the operation of the carry lookahead adder.
   (b) Design a 12-bit carry-select adder with 4-bit adders and MUXs.

6. (10%) What are the four steps in executing a MIPS instruction?

7. (10%) What are the relations between *cache*, *main memory*, and *virtual memory* in a memory hierarchy?

8. (6%) Explain the difference between *temporal locality* and *spatial locality*.

9. (6%) Explain the difference between *direct-mapped cache* and *fully associative cache.*

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10. 單選題(18%)

a. For a single-cycle design, which of the following statements is correct?
   (a) Each instruction is performed in one or more clock cycles.
   (b) The datapath resource can be used more than once for each instruction.
   (c) The clock cycle is determined by the shortest possible path in the implementation.
   (d) The signals within the datapath can vary unpredictably during a clock cycle.

b. For a multi-cycle design, which of the following statements is correct?
   (a) The execution time for each instruction is determined by the number of clock cycles it takes.
   (b) Each instruction is broken into a series of execution steps, and each step takes two clock cycles.
   (c) For each instruction, its CPI is equal to one.
   (d) The control information of an instruction has to travel with the instruction through the multi-cycle stages.

c. For a pipelined design, which of the following statements is correct?
   (a) For a five-stage pipeline, there will be five pipeline registers in the pipelined datapath.
   (b) Pipelining is a design technique in which multiple instructions are overlapped to be executed concurrently, and the number of overlapped instructions is equal to the number of pipeline stages.
   (c) Pipelining can decrease the execution time of an instruction when compared with the single-cycle design.
   (d) All the pipeline registers in a pipelined datapath are of the same length.

d. For the pipeline hazards, which of the following statements is correct?
   (a) The control hazard can be resolved by adding extra hardware to retrieve the missing item early from the internal resources.
   (b) Data hazards occur if the hardware cannot support the combination of instructions that we want to execute in the same clock cycle.
   (c) The load-use hazard cannot be resolved by forwarding after inserting a bubble instruction.
   (d) One solution to branch hazard is to stall immediately after a branch is fetched, i.e., waiting until the pipeline determines the outcome of the branch and knows what instruction address to fetch from.

e. For the page table design, which of the following statement is correct?
   (a) Each program can have its own page table.
   (b) A page table resides in the cache.
   (c) It is indexed with the page number from the physical address to discover the corresponding virtual page number.
   (d) It contains entries only for pages residing in memory.

f. For the virtual memory design, which of the following statements is correct?
   (a) Having a large number of physical pages than virtual pages is the basis for the illusion of an essentially unbounded amount of virtual memory.
   (b) When a page fault occurs, the miss penalty is dominated by the time to get the last word for typical page sizes.
   (c) The main memory acts as a “cache” for the secondary storage, usually implemented with magnetic disks.
   (d) The pages should be small enough to amortize the low access time.