國立彰化師範大學103學年度碩士班招生考試試題

系所：資訊工程學系(選考丁)、
電子工程學系(乙組選考乙)　　科目：計算機組織

☆☆請在答案紙上作答☆☆　　

1. (a) Describe Amdahl's Law and explain the meaning of Amdahl's Law.
   (b) Suppose you are trying to improve the performance of processor X, which spends 30% of its CPU time executing floating point (FP) operations and 16% of its CPU time executing load/store operations. The first improvement method is to make the FP operations run two times faster, and the second improvement method is to make the load/store run four times faster. Which method (the first or the second) can get higher speed-up?
   (c) Suppose the floating point (FP) operations can be improved by a factor of infinity, what is the speed-up? (15%)

2. Translate the following C code segment into MIPS assembly code

```
for (i=0; i<10; i++)
    {if (A[i] >= B[i])
        C[i] = A[i] - B[i];
     else
        C[i] = A[i] + B[i];
    }
```

   Assume variable ***i*** is already assigned to register ***R1***, the start address of integer array ***A*** is already stored in register ***R11***, the start address of integer array ***B*** is already stored in register ***R12,*** the start address of integer array ***C*** is already stored in register ***R13,*** and assume an integer occupies 4-byte memory. (15%)

3. Design a 3-bit ALU with the following specification. The ALU has two 3-bit inputs (***A*[2:0]** and ***B*[2:0]**), one 3-bit output (***Result*[2:0]**), and a 3-bit control (***OP*[2:0]**). When *OP*==000, *Result=A* OR *B*; when *OP*==001, *Result=A* AND *B*; when *OP*==010, *Result=A + B*; when *OP*==110, *Result=A – B*; when *OP*==111, *Result*=(*A* < *B*). Design this ALU using AND gates, OR gates, NOT gates, XOR gates, MUXs (multiplexer) and FAs (full adder). (10%)

4. Write a MIPS assembly code showing how to make a function call and how to make a function return. (10%)

5. What is the difference between direct-mapped cache, two-way set-associative cache, and fully associative cache? (10%)

6. Determine if each of the following statements is true (T) or false (F). (40%)

a. In the single-cycle design, the clock cycle time for all the instructions is determined by the delay of the fastest instruction.

b. In the multi-cycle design, the execution time for each instruction is determined by the number of clock cycles it takes.

c. For a Moore machine, the outputs depend on both the state bits and the inputs.

d. The ideal speedup due to pipelining is equal to the number of pipeline stages.

e. Pipelining improves performance by decreasing the execution time of each instruction.

f. The pipeline rate is determined by the slowest stage in the pipeline.

g. Data hazards arise from the dependence of one instruction on an earlier one that is still in the pipeline.

h. A method for resolving data hazards is to retrieve the missing item early from the internal resources, called forwarding.

i. The load-use data hazard can be resolved simply by forwarding.

j. Control hazards occur when the hardware cannot support the combination of instructions that we want to execute in the same clock cycle.

k. In the static branch prediction, the branch instruction can be assumed to be always taken or not taken.

l. With more hardware, the branch behavior can also be predicted dynamically during program execution.

m. Temporal locality means that if an item is referenced, items whose addresses are close to it will tend to be referenced soon.

n. The translation-lookaside buffer (TLB) is a memory that keeps track of recently used address translations.

o. For the least recently used (LRU) replacement scheme, a page that has not been used for a long time is less likely to be needed than a more recently accessed page.

p. When designing a virtual memory system, pages should be large enough to try to amortize the high access time.

q. Having a larger number of physical pages than virtual pages is the basis for the illusion of an essentially unbounded amount of virtual memory.

r. The page table resides in the cache and memory at the same time.

s. Page fault occurs when an accessed page is not present in the lowest-level hard disk.

t. The dirty bit is a bit in the page table to indicate whether a page needs to be copied back when we choose to replace it.