國立彰化師範大學 98 學年度碩士班招生考試試題

系所：電子工程學系　　組別：乙組　　科目：(乙)計算機組織

☆☆請在答案紙上作答☆☆　　

1. (15%) (a) The MIPS processor has an instruction JAL (Jump and Link). Describe the conditions in which you need to use the JAL instruction when writing a MIPS assembly program.
   (b) Describe the detailed hardware operations for the MIPS processor to execute a JAL instruction.

2. (15%) Describe at least three methods to reduce the branch penalty of a pipelined processor.

3. (15%) (a) Give two examples of false data dependence between instructions.
   (b) How to remove false data dependences between instructions?

4. (15%) Write the corresponding MIPS R2000 assembly codes for the following C code segment. Assume variable **i** is assigned to register *R1*; the start addresses of integer array **A** and **B** are already stored in register *R11*, *R12*; variable **sum** is assigned to register *R13*. An integer is 4-byte long.

```
// int A[10], B[10], sum;
while (i>=0){
      if(A[i]>=B[i])
            sum=sum+A[i];
      else
           sum=sum+B[i];
       i=i-1;
      }
```

5. (15%) A 3-bit ALU has two 3-bit inputs *A* and *B*, one 3-bit output *C*, and a 2-bit control input *S*. When *S* == 00, *C* = (*A* bitwise-AND *B*); when *S* == 01, *C* = (A bitwise-OR *B*); when S == 10, C= (A add B); when S == 11, C= (A subtract B). Use the basic logic gates (AND, OR, NOT, NAND, NOR, XOR), 1-bit full adders, and 1-bit 4-to-1 multiplexers to design the 3-bit ALU.

6. (15%) Assume that you have already finished the logic design of a single-cycle processor (i.e., the processor can complete the execution of an instruction within a single clock cycle). How to modify the logic design of a single-cycle processor into that of a five–stage pipelined processor? Give your answer in detail.

7. (10%) The instruction fetch unit (IFU) in a RISC processor takes charge of fetching instructions from memory to the instruction decoder. Plot the block diagram of IFU to show the internal architecture of (IFU), and illustrate how IFU deals with jump and branch instructions.