## 國立彰化師範大學 97 學年度碩士班招生考試試題

## 系所:<u>電子工程學系碩士班</u>組別:<u>乙組</u>

## ☆☆請在答案紙上作答☆☆

## 共1頁,第1頁

科目:計算機組織

1 • Interpret the following three types of dependency, and give an example for each type of $(150)$
(15%) (a) Read After Write dependency.
(a) <u>Read After White</u> dependency (b) Write After Read dependence
(c) Write After Write dependency
(c) <u>whice whice</u> dependency.
<ul> <li>2 (a) Plot the hardware diagram for the data forwarding scheme in pipelined processors</li> <li>(b) Can the data forwarding scheme remove the Load-Use data hazard? Give your reason. (15%)</li> </ul>
<ul> <li>3 A computer system has a <u>two-way set-associative</u> data cache. This data cache has 1024 blocks in total and each block contains 16 bytes. Plot the hardware diagram for this data cache. You must show how the address from the processor is used to select one data item out of the cache. (15%)</li> </ul>
4 • Write the corresponding MIPS R2000 assembly codes for the following C code segment. (Assume
variable i is assigned to register R1, and the start addresses of array A, B, and C, are already stored
in register R11, R12, R13. An integer is 4-byte long.) (15%)
// int A[10], B[10], C[10];
while (i>=0){
if(B[i]>=C[i])
$\mathbf{A}[\mathbf{i}] = \mathbf{B}[\mathbf{i}] + \mathbf{A}[\mathbf{i}];$
else
A[1]=C[1]+A[1]; ;_; 1.
1=1-1;
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- 5 Explain how a processor handles interrupts and exceptions. Describe a exception handling mechanism for the processor so that the processor can jump to the corresponding exception handling routine and can resume the execution of the interrupted program after the exception handling routine is executed. (15%)
- 6 Describe the Booth's Algorithm for multiplication. Use the Booth's Algorithm to compute 10110110x11110110 step by step. (15%)
- 7 Interpret the <u>big-endian scheme</u> and the <u>little-endian scheme</u>. If a 32-bit data, 0xd75afb68, is stored in memory from address 100 to address 103, what is the memory content at address 101 for each scheme?