1. (10%) Write the corresponding MIPS R2000 assembly codes for the following C code segment. (Assume variable i is assigned to register R1, and the start addresses of array A, B, C, and D, are already stored in register R11, R12, R13, R14. An integer is 4-byte long.)
   // int A[10], B[10], C[10], D[10];
   for (i=0;i<=9;i++){
   　　if(B[i]>=C[i])
   　　 A[i]=B[i]+D[i];
   　　else
   　　　A[i]=C[i]+D[i];
   　　}

2. (10%) (a) What is TLB (Translation-lookaside buffer)? Plot the internal architecture of TLB and interpret how TLB operates.
   (b) What should the computer system do when it suffers a TLB miss?

3. (10%) Interpret structural hazards and give at least three examples of structural hazards.

4. (10%) Plot the internal architecture of the branch unit for a RISC processor, and interpret how the branch unit processes a branch instruction.

5. (10%) (a) When does an overflow occur for integer addition/subtraction?
   (b) Design the circuit of overflow detection for a 4-bit ALU with addition/subtraction.

6. (10%) Compare the differences between VLIW (Very Long Instruction Word) and superscalar processors in detail.

7. (10%) (a) Interpret caller-saved registers and callee-saved registers.
   (b) Interpret the function of the link register.

8. (10%) Interpret the meanings of Amdahl's law in detail.

9. (10%) Interpret write-through cache and write-back cache, respectively, and compare their differences.

10. (10%) Interpret false data dependency and give at least two methods to eliminate false data dependency.