

國立彰化師範大學 98 學年度碩士班招生考試試題

系所：電子工程學系

組別：乙組

科目：(甲)邏輯設計

☆☆請在答案紙上作答☆☆

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- Using the 2's complement to compute the differences of the following expressions? 10%
 - $01011 - 01110$
 - $101011 - 011001$

- Show a truth table (refer to Fig. 1) for a 2-bit subtractor that has a minuend input x_1x_0 and a subtrahend y_1y_0 , and produces a difference d_1d_0 , and a borrow b_{out} . 10%

$x_1x_0y_1y_0$	$b_{out}d_1d_0$
0 0 0 0	⋮
⋮	⋮

Fig. 1 Truth table example

- Simplify the following function expressions by algebraic manipulation 10%
 - $F(A, B, C, D) = (A + B + C)(B + C + D)(A' + C + D)(B' + C' + D')$
 - $F(A, B, C, D) = A'BC' + BC'D' + A'CD + B'CD + A'BD$
- Referring to the function $F(w, x, y, z) = (w + x + y + z')(x + y + z)(x' + y')$
 - Derive the SOP (Sum of Product) and POS (Product of Sum) canonical forms 5%
 - Simplify the function using the Karnaugh map 5%
- Using the 8-to-1 multiplexer (as shown in Fig. 2) to realize the following function 5%

$$F(A, B, C, D) = BD + B'C + AB'$$
- Using several 2-to-4 decoders (referring to Fig. 3) with additional input EN(Enable) to design a 4-to-16 decoder? 5%

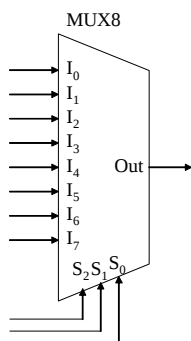


Fig. 2 8-to-1 multiplexer

EN	A	B	Y0	Y1	Y2	Y3
0	x	x	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Fig. 3 2-to-4 decoder with additional input EN

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7. Sequential circuits M1 and M2 have the state tables depicted in Tab. 1 and Tab. 2, determine whether the sequential circuits M1 and M2 are equivalent? 10%

Tab. 1 M1 state table

	Next state		Output	
	$x=0$	1	$x=0$	1
A	B	A	0	0
B	C	D	0	1
C	A	C	0	1
D	C	B	0	0

Tab. 2 M2 state table

	Next state		Output	
	$x=0$	1	$x=0$	1
S_0	S_3	S_1	0	1
S_1	S_3	S_0	0	0
S_2	S_0	S_2	0	0
S_3	S_2	S_3	0	1

8. Show a state diagram for the state table in Tab. 3? 10%

Tab. 3

	Next state				Output
	$xy=00$	01	10	11	
a	a	c	e	d	0
b	d	e	e	a	0
c	e	a	f	b	1
d	b	c	c	b	0
e	c	d	f	a	1
f	f	b	b	d	1

9. Design a sequential circuit using JK flip-flops for state table in Tab. 4 and state assignment: A = 00, B = 01, C = 11, and D = 10? 10%

Tab. 4

	Next state		Output
	$x=0$	1	
A	B	D	0
B	C	A	1
C	B	B	1
D	D	C	1

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10. Reduce the state table in Tab. 5 to a minimum number of states, and draw the state graph of the reduced state table? 10%

Tab. 5

	Next state		Output	
	x=0	1	x=0	1
A	B	C	1	0
B	E	D	1	0
C	G	D	1	1
D	E	B	1	0
E	F	G	1	0
F	H	B	1	1
G	H	I	0	1
H	G	I	0	1
I	A	a	0	1

11. Derivate the state graph of the sequential circuit in Fig. 4? 10%

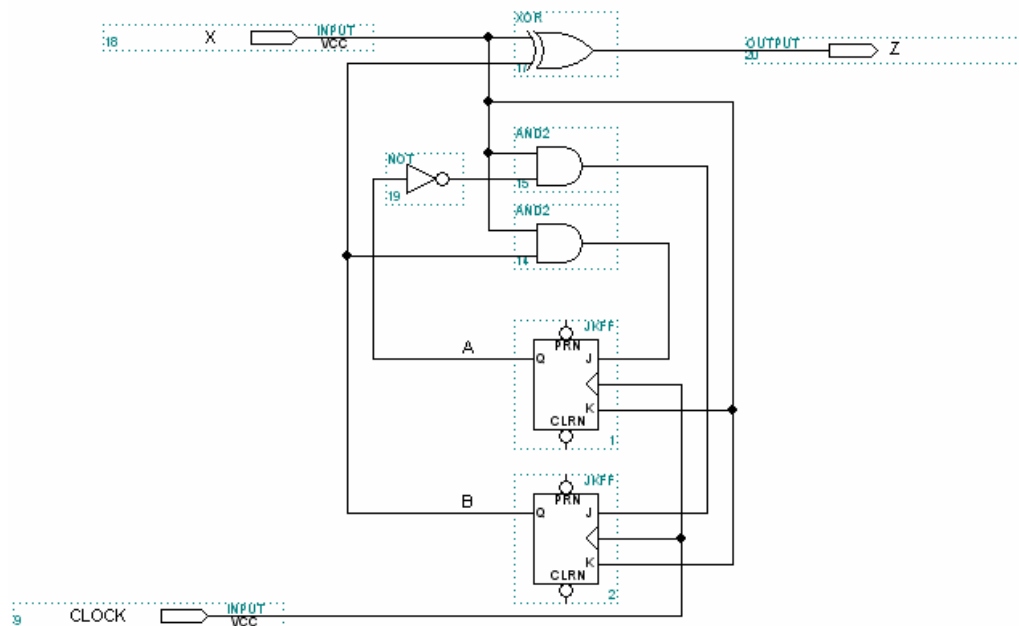


Fig. 4 sequential circuit