

國立彰化師範大學 97 學年度碩士班招生考試試題

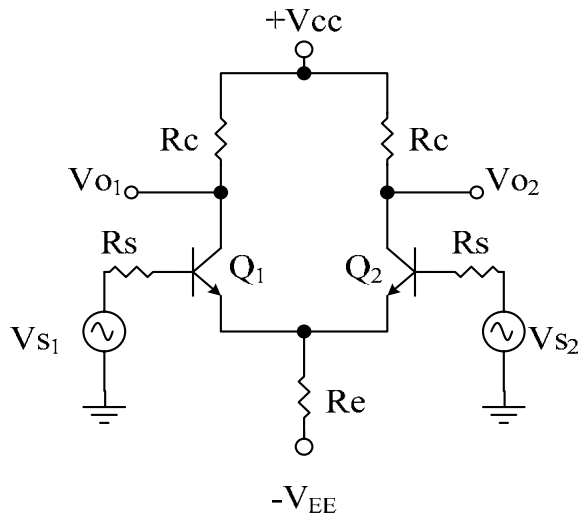
系所：積體電路設計研究所碩士班

科目：電子學

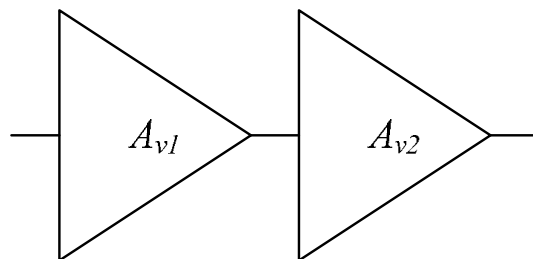
☆☆請在答案紙上作答☆☆

共 3 頁，第 1 頁

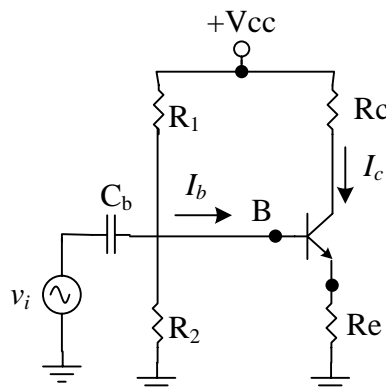
1. (20%) Given the same h -model parameters h_{fe} , h_{ie} , h_{oe} for differential pair Q_1 and Q_2 as follows, derive the difference-mode gain A_d and common-mode gain A_c . While mapping the BJT technology to MOS technology, describe the major pros and cons briefly.



2. (15%) For a 2-stage amplifier with voltage gains A_{v1} and A_{v2} prior to compensation, assume that the effective load from the collector of stage 1 is R_L and the associated (dc gains, and dominant poles) are (A_{vo1}, f_1) and (A_{vo2}, f_2) separately. Redraw the compensated circuit by adding a feedback capacitor, C_f , for a typical Miller-effect compensation. Find the compensation frequency f_{1c} .



3. (15%) Given an emitter-biased amplifier with $\beta=50$, $V_{CC}=20V$, $R_C=4.7k\Omega$, $R_E=1k\Omega$, $R_1=90k\Omega$, and $R_2=10k\Omega$. V_{BE} is assumed to be $0.7V$. Find the Q operational point, (I_C, I_B, V_{CE}) .



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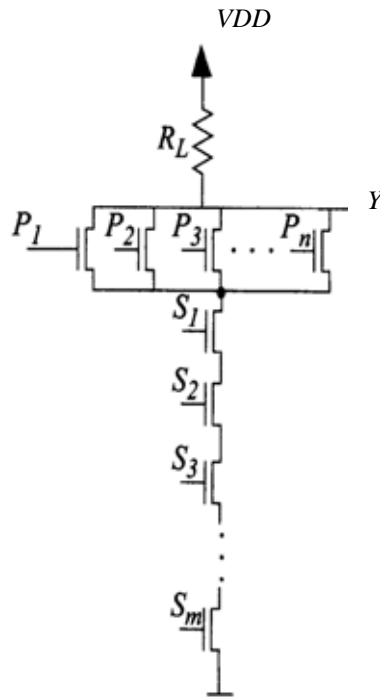
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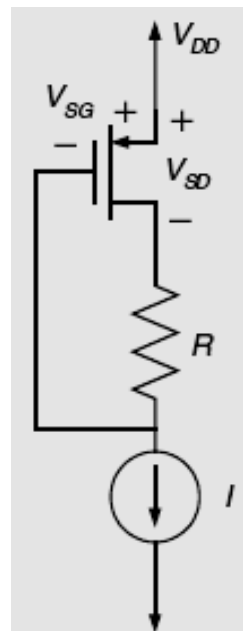
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共 3 頁，第 2 頁

4. (15%) The digital circuit below has logic inputs $P_1, P_2, \dots, P_n, S_1, S_2, \dots, S_m$ and output Y . Assuming that the element values are chosen so that the circuit satisfies a static discipline, what is the logic function computed by the circuit?



5. (20%) For the circuit shown below, a.(10%) Find the range of R that would keep the p-channel MOSFET in saturation. b.(10%) Determine V_{SG} when the MOSFET is in saturation. Describe V_{SG} by V_{th}, W, L , etc.



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共 3 頁，第 3 頁

6. (15%) The circuit below is a voltage divider composed of three diode-connected Enhancement MOSFET. Utilizing a current $I = 90\mu\text{A}$, find the W/L ratios of the three transistors, so that the divider provides $V_1 = 1\text{V}$ and $V_2 = -1\text{V}$. Let $V_T = 1\text{V}$ and $\mu_n C_{ox} = 20\mu\text{ A/V}^2$. Neglect the small effect of r_o of each of the three devices.

