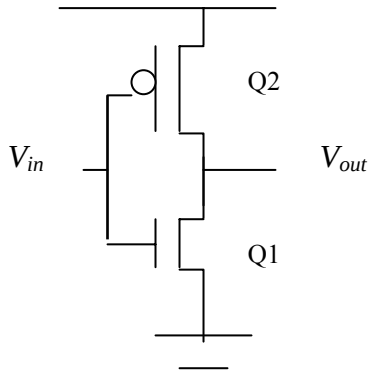
# 國立彰化師範大學九十六學年度碩士班招生考試試題

系所：積體電路設計研究所　　科目： 電子學

☆☆請在答案紙上作答☆☆　　

1. (25%) $K_p\,(enh)$ = 12.5 × $10^{-6}$ amps/volt$^2$, $K_n\,(enh)$ = 25 × $10^{-6}$ amps/volt$^2$, $V_{tn}\,(enh)$ = 1 V for Q1, $V_{tp}\,(enh)$ = -1 V for Q2, W/L (Q2 ) = 1, W/L (Q1) = 1, Q1 and Q2 are both enhancement transistors. For a 5 V supply voltage, find the transfer characteristics ($V_{in}$ vs. $V_{out}$) with $V_{in}$ varying from 0 to 5 volts and plot it on the paper. Be sure to label all transition points such as turn on, Sat/Unsat for all transistors.




2. (20%) For a junction, the acceptor concentration is $10^{16}$cm$^{-3}$ and the donor concentration is $10^{15}$ cm$^{-3}$, find the junction built-in voltage. Assume $n_i \approx 10^{10}$cm$^{-3}$. Also find the width of the depletion region ($W_{dep}$) and its extent in each of the *p* and *n* regions when the junction is reversed biased with $V_R$ = 5 V. At this value of reversed biased, calculate the magnitude of the charge stored on either side of the junction. Assume the junction area is 400 $\mu$m$^2$. Also calculate $C_j$.

3. (10%) The physical origin of the forward "Early effect" is (a) A reduction in base width due to base-collector junction bias. (b) Higher electric fields at high bias voltages. (c) Base-collector junction leakage. (d) Increased efficiency of the collector. (e) Reduction in base width due to emitter-base bias.

4. (10%) Which of the following is **not true**? (a) A large Early voltage corresponds to a small Early effect. (b) The forward and reverse Early voltages are in general different. (c) The forward Early voltage may be expressed in terms of the collector-base junction capacitance. (d) The Early voltage is directly proportional to collector current. (e) The Early voltage is primarily determined by manufacturing methods.

5. (10%) Which of the following is **not true**? (a) $\beta_F$ is a function of emitter current. (b) $\beta_F$ falls off at low values of collector current. (c) $\beta_F$ falls off at high values of collector current. (d) $\beta_F$ fall off is due to carrier generation in the emitter-base space charge region. (e) $\beta_F$ fall off at high current can be delayed by proper device structure.

6. (25%) An NMOS transistor, operating in the linear-resistance region with $v_{DS}$ = 0.1 V, is found to conduct 40 $\mu$A for $v_{GS}$ = 2 V and 80 $\mu$A for $v_{GS}$ = 3 V. What is the apparent value of threshold voltage $V_t$? If $k_n$' = 40 $\mu$A/V$^2$, what is the device W/L ratio? What current would you expect to flow with $v_{GS}$ = 2.5 V and $v_{DS}$ = 0.15 V? If the device is operated at $v_{GS}$ = 2.5 V, at what value of $v_{DS}$ will the drain-end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?