

# 國立彰化師範大學 99 學年度碩士班招生考試試題

系所：電信工程學研究所

組別：選考甲

科目：電子學

☆☆請在答案紙上作答☆☆

共 2 頁，第 1 頁

1. Fig. 1 is a two-pole low-pass filter. Find the transfer function  $T(s) = V_o(s)/V_i(s)$ , where  $s = j\omega$ . (15%)
2. For the common-emitter amplifier shown in Fig. 2, let  $V_{CC} = 9\text{ V}$ ,  $R_1 = 27\text{ k}\Omega$ ,  $R_2 = 15\text{ k}\Omega$ ,  $R_{E1} = 0.2\text{ k}\Omega$ ,  $R_{E2} = 1\text{ k}\Omega$ , and  $R_C = 2.2\text{ k}\Omega$ . The BJT has  $\beta = 100$  and  $V_A = 100\text{ V}$ . Calculate the dc bias current  $I_E$ . If the amplifier operates between a source for which  $R_s = 10\text{ k}\Omega$  and a load of  $R_L = 2\text{ k}\Omega$ , replace the BJT with its hybrid- $\pi$  model, and find the values of  $R_{in}$  and the voltage gain  $v_o/v_s$ . (20%)
3. Consider the common-source n-MOSFET amplifier shown in Fig. 3 with threshold voltage  $V_{th} = 1.8\text{ V}$ , conduction parameters  $k_n = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} = 0.15\text{ mA/V}^2$ , and  $\lambda = 0$ . (a) Calculate dc bias current  $I_D$  and voltage  $V_D$ . (b) Determine the small signal voltage gain. (c) Discuss the purpose of  $R_G$  and its effect on the small-signal operation of the amplifier. (Assume  $C_{C1}$  and  $C_{C2}$  are large enough for ac operation.) (15%)

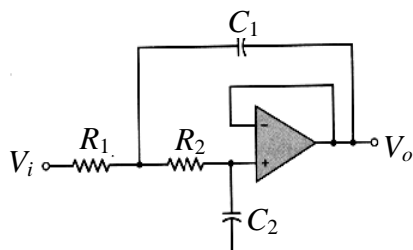


Fig. 1

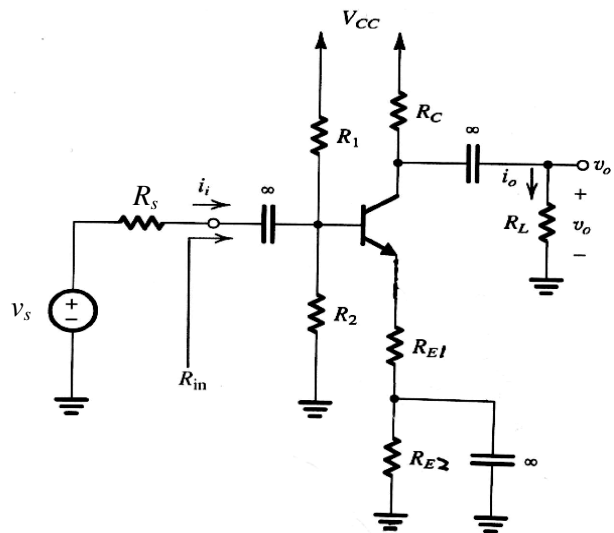


Fig. 2

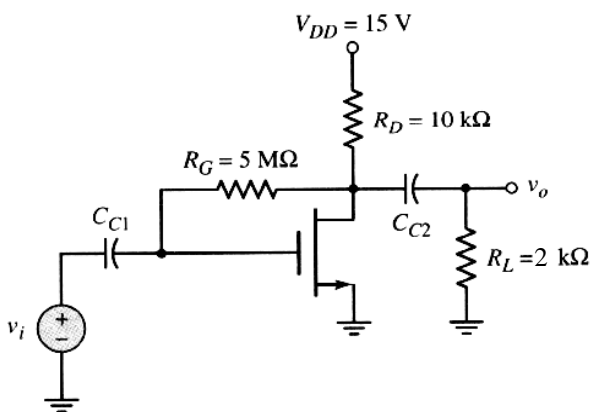


Fig. 3

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4. (a) Sketch a two inputs NOR gate of the pseudo NMOS logic structure. (7%)  
 (b) What are the advantages and disadvantages of pseudo NMOS logic when it compared with CMOS logic? (8%)
5. Fig. 4 shows the circuit for determining the output resistance when  $v_{out}$  is positive and  $Q_3$  is conducting most of the current. Neglecting the large output resistance of  $Q_1$ , find  $R_o$  when  $Q_3$  is sourcing an output current of 2 mA. (The bias current of  $Q_1$  is  $300 \mu\text{A}$ ,  $I_{sn}=10^{-14}\text{A}$ ,  $\beta_n=100$ ,  $V_{an}=125\text{V}$ ,  $I_{sp}=10^{-14}\text{A}$ ,  $\beta_p=50$ ,  $V_{ap}=50\text{V}$ )(15%)
6. For the circuit in Fig. 5  $|V_t| = 1\text{V}$ ,  $k'W/L = 1\text{mA/V}^2$ ,  $h_{fe} = 100$ , and the Early voltage magnitude for all devices (including those that implement the current sources) is  $80\text{V}$ . The signal source  $V_s$  has a zero dc component. Find the dc voltage at the output and at the base of  $Q_3$ (3%). Find the values of  $A$ (4%),  $\beta$ (4%),  $A_f$ (3%),  $R_{in}$  (3%) and  $R_{out}$ (3%).

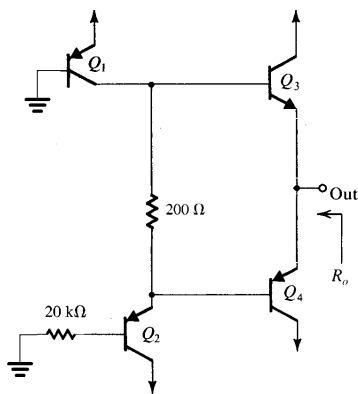


Fig. 4

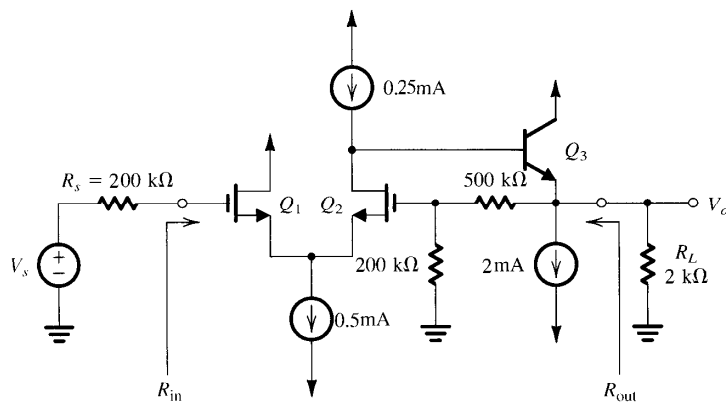


Fig. 5